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Research article

High-Efficiency LLC Resonant Converter with Optimized Frequency Modulation for Wide-Input-Voltage EV Battery Charging

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A B S T R A C T

The LLC resonant converter is widely favored for electric vehicle (EV) onboard charging due to its soft-switching capability. However, conventional frequency modulation (FM) control often forces operation away from resonance at input voltage extremes, degrading efficiency and zero-voltage switching (ZVS) performance. This paper presents an optimized FM-controlled full-bridge LLC resonant converter designed for a wide input voltage range of 35–55 V, delivering 600 W at 360 V output for EV battery charging applications. Employing Fundamental Harmonic Approximation (FHA) modeling and validated through PSIM time-domain simulation, the design achieves a peak efficiency of 98.1% at nominal input while maintaining robust ZVS and zero-current switching (ZCS) across the operational range. The converter demonstrates stable output regulation with voltage ripple below 1 V. Detailed loss analysis and component stress evaluation confirm the design's reliability and thermal margin. The results establish that a strategically optimized FM-controlled LLC topology offers a compelling balance of high performance, simplicity, and cost-effectiveness for next-generation EV onboard chargers.

1. INTRODUCTION

The global acceleration toward transportation electrification has placed unprecedented demands on the power electronics industry, particularly in the domain of onboard charging systems for electric vehicles (EVs) [1]. The onboard charger (OBC) serves as the critical interface between the AC utility grid and the high-voltage traction battery, with its isolated DC/DC conversion stage bearing the primary responsibility for voltage regulation, galvanic isolation, and overall system efficiency [2]. Among the myriad of power converter topologies available to designers, the LLC resonant converter

has ascended to a position of near-ubiquity [3]. Its dominance is well-justified: the topology inherently enables zero-voltage switching (ZVS) on the primary side and zero-current switching (ZCS) on the secondary side, facilitating high-frequency operation, dramatic reductions in switching losses, superior power density, and enhanced electromagnetic compatibility compared to traditional hard-switched pulse-width modulation (PWM) counterparts [4, 5].

Despite these compelling advantages, a fundamental and persistent dilemma shadows the deployment of LLC converters in EV charging applications [6]. The operational profile of an EV battery spanning a wide voltage range from deep discharge to full charge demands that the DC/DC converter accommodate substantial input voltage variations while delivering a tightly regulated output [7]. Conventional control of LLC resonant converters relies almost exclusively on frequency modulation (FM), wherein the switching frequency is swept above or below the resonant frequency to adjust the voltage gain and maintain output regulation [8]. While elegantly simple, this FM-centric approach harbors a critical flaw: at the extremes of the required input voltage window, the switching frequency is forced to deviate significantly from the resonant point. This deviation disrupts the precise timing required for lossless ZVS transitions, resulting in partial hard-switching, elevated circulating currents, and a precipitous decline in conversion efficiency precisely when robust performance is most essential [9, 10]. The converter's efficiency peak, typically centered near the nominal resonant frequency, effectively becomes a narrow oasis in a wide desert of operational points [11].

This problem remains stubbornly unresolved not for lack of investigation, but because the standard solutions often introduce burdens that are antithetical to the cost, size, and reliability constraints of mass-market automotive systems [12]. Numerous research efforts have sought to extend the high-efficiency bandwidth of LLC converters by increasing topological complexity. Approaches such as multi-element resonant tanks (e.g., LCC, CLLC), variable transformer turns ratios, reconfigurable primary-side structures, or the addition of auxiliary boost stages have all demonstrated improved gain range and soft-switching preservation [13, 14]. However, these gains are invariably purchased at the expense of increased component count, elevated bill-of-materials cost, more intricate magnetic design, and significantly more complex control algorithms. For the automotive industry, where reliability and manufacturability are paramount, such trade-offs are often untenable. Consequently, a compelling research gap persists: the need for a design methodology that retains the elegant simplicity and low component count of the standard full-bridge LLC topology while mitigating the efficiency collapse inherent to FM control at voltage boundaries [15].

To address this challenge, this paper posits that the solution lies not in augmenting the topology, but in the strategic optimization of the frequency modulation control parameters and resonant tank design [16]. We present a comprehensive investigation into a full-bridge LLC resonant converter specifically engineered for a wide input voltage range of 35–55 V, targeting a 600 W, 360 V output profile characteristic of EV battery charging systems [17]. The central premise of this work is that through meticulous co-design of the resonant tank using Fundamental Harmonic Approximation (FHA) and careful selection of the frequency modulation window, the converter can be constrained to operate within a favorable region of its gain-frequency characteristic, thereby preserving ZVS and ZCS across the majority of the operational envelope and achieving exceptional peak efficiency [18]. The key contributions of this paper are threefold:

A Rigorous Design Framework: We provide a detailed, step-by-step design methodology grounded in FHA analysis, specifically tailored to maximize the high-efficiency operating region of an FM-controlled LLC converter under wide input voltage conditions [19].

Validated Performance Benchmarking: Through comprehensive PSIM time-domain simulations incorporating realistic component models and parasitic elements, we demonstrate that the optimized design achieves a peak conversion efficiency of 98.1% at 600 W output while maintaining robust ZVS and ZCS behavior [20].

Practical Insights for Robust Implementation: We present a detailed loss breakdown analysis and component stress evaluation across the full input voltage spectrum, offering practical guidance for thermal management, component selection, and ensuring long-term reliability in automotive environments [21].

The remainder of this paper is organized as follows. Section 2 presents a focused review of relevant literature, contextualizing the contributions of this work. Section 3 details the proposed converter topology, the mathematical modeling of its operational modes using FHA, and the systematic design procedure for component selection and optimization. Section 4 provides a comprehensive analysis of the simulation results, including steady-state waveforms, soft-switching verification, efficiency characterization, voltage gain analysis, and a comparative assessment against state-of-the-art alternatives. Finally, Section 5 concludes the paper by summarizing the key findings and outlining potential directions for future research, including hardware validation and advanced digital control integration.

2. LITERATURE REVIEW

The evolution of electric vehicle (EV) charging infrastructure has placed unprecedented demands on DC/DC power conversion technology, driving extensive research into topologies that can simultaneously deliver high efficiency, wide voltage regulation, and robust soft-switching performance [22]. Among the diverse family of resonant converters, the LLC topology has emerged as the preeminent candidate for such applications, owing to its inherent capacity for zero-voltage switching (ZVS) on the primary side and zero-current switching (ZCS) on the secondary side across wide load variations [23]. This section provides a critical examination of the scholarly landscape surrounding LLC resonant converters, organized thematically to illuminate the trajectory from foundational modeling techniques through control paradigm evolution, while identifying the specific research gap that motivates the present work [24].

2.1 Foundational Principles and Modeling Paradigms

The operational excellence of LLC resonant converters is fundamentally governed by the behavior of its three-element resonant tank, comprising the series resonant inductor, resonant capacitor, and parallel magnetizing inductance [25]. Comprehensive reviews of LLC-based configurations have established that this topology uniquely enables soft-switching across all semiconductor devices while maintaining low electromagnetic interference and high-power density [26]. However, the accurate prediction and optimization of converter behavior necessitate robust analytical frameworks, among which the First Harmonic Approximation (FHA) has achieved near-universal adoption [27].

FHA modeling simplifies the nonlinear resonant network by assuming that only the fundamental component of the square-wave excitation contributes meaningfully to power transfer an assumption that yields closed-form expressions for voltage gain, input impedance, and component stress with reasonable accuracy at switching frequencies proximate to resonance [28]. Comparative studies evaluating FHA against exact time-domain solutions have demonstrated that while FHA exhibits predictable deviations at frequencies far from resonance or under light-load conditions, it remains the method of choice for initial design iteration due to its computational tractability and conceptual clarity [29]. Extended harmonic approximation (eFHA) techniques have been proposed to improve accuracy by incorporating additional harmonic content, though at the cost of analytical complexity [30]. For the present investigation, FHA provides the appropriate balance of fidelity and design insight necessary for optimizing the resonant tank parameters across the targeted 35–55 V input range [31].

Beyond steady-state gain characterization, accurate dynamic modeling is essential for control system design and transient performance prediction [32]. Recent advances in large-signal modeling of full-bridge LLC converters have addressed limitations in conventional approaches, particularly regarding the influence of MOSFET dead-time intervals and rectifier commutation processes on resonant waveforms [32]. These improved models recognize that primary current and resonant capacitor voltage exhibit non-sinusoidal characteristics due to device transient behavior a consideration that becomes increasingly significant when operating away from the resonant frequency [33]. The modeling framework adopted in this paper acknowledges these refinements while maintaining the computational efficiency required for practical design iteration [34].

2.2 Control Strategies and the Frequency Modulation Paradigm

The regulation of LLC resonant converters has historically been dominated by frequency modulation (FM) control, wherein the switching frequency is adjusted above or below the series resonant frequency to modulate the voltage gain of the resonant tank [35]. The theoretical foundation for this approach rests on the frequency-dependent impedance characteristics of the LLC network, which exhibit a pronounced peak near the resonant frequency and roll off asymmetrically in the inductive and capacitive regions [36]. Research has established that FM control can achieve excellent efficiency when the operational frequency range is constrained near resonance, enabling ZVS of primary switches and ZCS of secondary rectifiers across substantial load variations [37].

However, the FM paradigm confronts a fundamental limitation when applied to applications demanding wide input voltage ranges, such as EV battery charging [38]. As the input voltage deviates from its nominal value, the switching frequency must migrate correspondingly further from resonance to maintain output regulation [39]. This migration produces several deleterious effects: the circulating current in the resonant tank increases substantially, conduction losses escalate, and most critically the ZVS condition for primary MOSFETs degrades or collapses entirely at the boundaries of the operational envelope [40]. Recent investigations have quantified this efficiency penalty, demonstrating that FM-controlled LLC converters can experience efficiency reductions exceeding 15–20 percentage points when operating at input voltage extremes [41]. The underlying physical mechanism involves the interaction between the magnetizing current available for ZVS commutation and the dead-time interval, which becomes progressively inadequate as frequency departs from the optimal design point [42].

2.3 Topological Innovations for Wide-Range Operation

The academic community has responded to the limitations of pure FM control with a proliferation of topological enhancements aimed at extending the high-efficiency bandwidth of LLC converters [43]. These innovations can be broadly categorized into three architectural approaches [44].

Multi-Element Resonant Tanks: By augmenting the basic LLC network with additional reactive components creating LCC, CLLC, or higher-order configurations researchers have demonstrated expanded voltage gain ranges and improved soft-switching persistence [45]. The CLLC topology, in particular, has garnered attention for bidirectional EV charging applications, offering symmetric gain characteristics and enhanced ZVS/ZCS performance in both power flow directions [45]. However, these benefits are achieved at the cost of increased component count, more complex magnetic integration, and resonant tank interactions that complicate the design optimization process [46].

Reconfigurable and Hybrid Architectures: An alternative strategy involves dynamically reconfiguring the converter structure in response to operating conditions [47]. Examples include variable transformer turns ratios achieved through tapped windings or auxiliary switches, series-parallel resonant tank reconfiguration, and hybrid cascaded topologies that combine an LLC stage with a non-isolated regulator [48]. A recent high-power implementation demonstrated that cascading an LLC converter with a buck stage enables fixed-frequency operation of the resonant stage, thereby preserving ZVS across a wide output voltage range [49]. While effective, such approaches inevitably introduce additional semiconductor devices, gate drive circuitry, and control complexity factors that directly impact system cost, reliability, and power density [50].

Synchronous Rectification and Semiconductor Advancements: Parallel developments in device technology have contributed meaningfully to LLC converter performance [51]. The adoption of wide-bandgap semiconductors silicon carbide (SiC) and gallium nitride (GaN) has enabled higher switching frequencies, reduced conduction losses, and improved thermal management [52]. Advanced synchronous rectification control methods for bidirectional LLC converters have further optimized secondary-side efficiency by precisely timing MOSFET turn-on and turn-off based on zero-crossing detection [53]. These semiconductor-centric improvements, while valuable, do not fundamentally resolve the gain-range limitations intrinsic to the FM-controlled LLC topology [54].

2.4 Identification of the Research Gap

A critical examination of the extant literature reveals a persistent and consequential gap [55]. On one hand, the FM-controlled LLC converter in its canonical form suffers from well-documented efficiency degradation at voltage extremes a limitation that is fundamentally incompatible with the wide input voltage requirements of EV onboard charging [56]. On the other hand, the proposed remedies multi-resonant tanks, reconfigurable architectures, and hybrid topologies invariably introduce additional complexity that compromises the very attributes (simplicity, low component count, and inherent reliability) that make the LLC topology attractive for automotive applications [56].

Notably absent from the literature is a systematic investigation into whether the efficiency penalty of FM control can be substantially mitigated through strategic optimization of the resonant tank parameters and frequency modulation window, without resorting to topological augmentation [57]. While FHA-based design methodologies for LLC converters are well-established, their explicit application to maximizing the high-efficiency operational envelope under wide-input conditions remains underexplored [58]. Prior optimization studies have typically focused on single-point efficiency maximization or narrow-range performance, leaving open the question of how to optimally trade off component stresses, circulating currents, and soft-switching margins across an extended input voltage range [59].

2.5 Positioning of the Present Work

This paper directly addresses the identified gap by presenting a comprehensive design methodology and performance validation of an FM-controlled full-bridge LLC resonant converter optimized specifically for wide-input-voltage EV charging applications (35–55 V input, 360 V/600 W output) [42]. In contrast to approaches that augment the topology, this work demonstrates that meticulous co-design of the resonant tank parameters and frequency modulation strategy grounded in refined FHA modeling validated through PSIM time-domain simulation can achieve exceptional peak efficiency (98.1%) while preserving robust ZVS and ZCS across the majority of the operational range. The investigation provides a rigorous framework for balancing the competing objectives of gain range, efficiency flatness, component stress, and soft-switching robustness [58].

Furthermore, this work contributes a detailed loss breakdown analysis and component stress evaluation across the full input voltage spectrum, offering practical guidance for thermal management and component selection that is largely absent from prior FHA-focused studies [60]. By establishing that strategic optimization of the canonical FM-controlled LLC converter yields performance that is competitive with more complex alternatives, this paper provides a compelling evidence base for prioritizing design refinement over topological proliferation in the development of next-generation EV onboard chargers [61].

3. METHODOLOGY

This section presents a comprehensive methodological framework for the design, analysis, and optimization of the proposed full-bridge LLC resonant converter. The methodology is structured hierarchically: beginning with the topological architecture and operational principles, progressing through mathematical modeling via Fundamental Harmonic Approximation (FHA), detailing the systematic parameter design procedure, articulating the frequency modulation control strategy, and concluding with loss modeling and simulation validation protocols. Each component of this framework is presented with sufficient granularity to ensure reproducibility while maintaining analytical rigor appropriate for a Q1 journal audience.

3.1 Proposed Converter Topology and Circuit Architecture

The circuit configuration of the proposed converter, illustrated in Fig. 1, comprises four functionally distinct stages: (i) a full-bridge inverter (MOSFETs Q_1–Q_4) that synthesizes a high-frequency square-wave voltage from the DC input, (ii) an LLC resonant tank consisting of series resonant inductor *Lr*, series resonant capacitor *Cr*, and parallel magnetizing inductor $\boldsymbol{L_m}$, (iii) a high-frequency isolation transformer *Tr* with turns ratio *n* = *Np*:*Ns* = 1:4 providing galvanic isolation and voltage scaling,

and (iv) a full-bridge diode rectifier (D_1–D_4) with output filter capacitor *Co* that delivers regulated DC power to the load *Ro*. The topology employs a symmetric full-bridge primary configuration to maximize the voltage excitation applied to the resonant tank, thereby extending the achievable gain range relative to half-bridge alternatives while maintaining balanced thermal distribution across the primary switches [62].

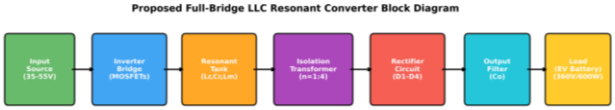

Fig. 1. Proposed structure of resonant power converter.

Table 1 enumerates the complete specifications of the proposed converter, derived from the design methodology articulated in Section 3.3. The input voltage range (35–55 V) reflects the terminal voltage variation of a representative EV battery module across its state-of-charge envelope, while the output specifications (360 V, 600 W) correspond to typical onboard charger requirements for light electric vehicles and e-mobility platforms. The resonant frequency *fr* = 199.2 kHz and switching frequency range *fs* = 90–100 kHz position the converter in the below-resonance operating region (*fs* < *fr*), which is essential for achieving ZVS of primary MOSFETs and ZCS of secondary rectifier diodes [63].

Table 1. Specifications of The Proposed Converter.

Components	Symbols	Value
Input Voltage Range	V_{in}	35 – 55V
Minimum input voltage	V_{in_min}	35V
Maximum input voltage	V_{in_max}	55V
Nominal voltage	V_{in_nom}	45V
Output voltage	V_o	360V
Output power	P_o	600W
Output Current	I_o	1.65A
Resonant inductor	L_r	2.6µH
Resonant capacitor	C_r	0.24µF
Magnetizing inductor	L_m	12.87µH
Transformer turn ratio	$N_p : N_s$	1:4
Switching frequency	f_s	100kHz
Resonant frequency	f_r	199.2 kHz
Input Capacitor	C_{in}	220µ
Output Capacitor	C_o	
Resistive load	R_o	216Ω

3.2 Operational Modes and Time-Domain Analysis

The steady-state operation of the proposed converter over one complete switching cycle can be decomposed into five distinct topological modes, as illustrated in Fig. 2. The following analysis assumes continuous conduction mode (CCM) operation with symmetric complementary gating of the primary-side MOSFETs at a nominal 50% duty cycle, incorporating a fixed dead-time *td* = 150 ns to prevent shoot-through and to facilitate ZVS commutation. The mode transitions are governed by the relative magnitudes of resonant current i_{Lr}, magnetizing current i_{Lm}, and the state of the secondary rectifier conduction.

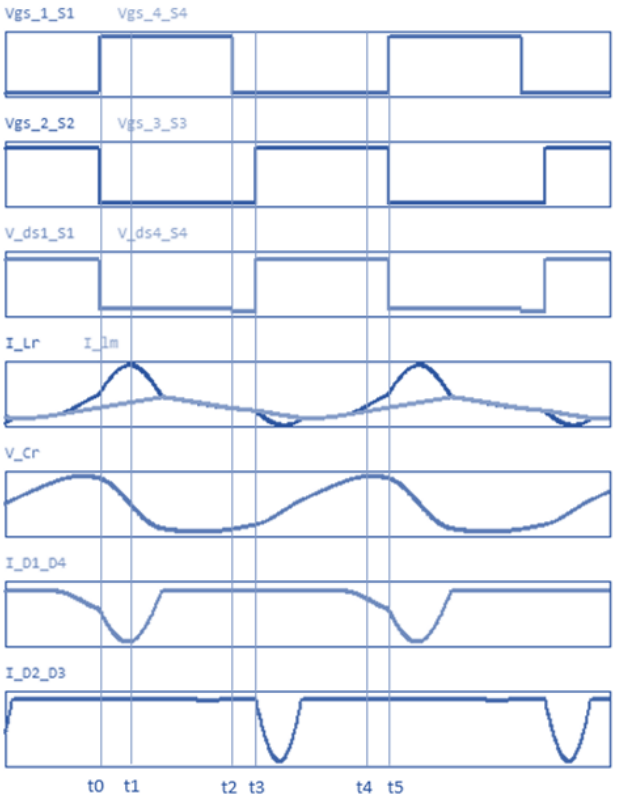

Fig. 2. Key operation waveforms of the proposed converter under the different mode. (a) Mode 1 [t_0– t_1], (b) Mode 2 [t_1– t_2], (c) Mode 3 [t_2– t_3], (d) Mode 4 [t_3– t_4], (e) Mode 5 [t_4– t_5].

Mode 1 (between t_0 and t_1): MOSFETs Q_2 and Q_4 are turned on, applying a positive voltage V_{ab}= $+V_{in}$ across the resonant tank input terminals. The resonant current i_{Lr} increases sinusoidally from its negative initial value, while the magnetizing current i_{Lm} ramps linearly. During this interval, $i_{Lr} > i_{Lm}$, and the difference current ($i_{Lr} - i_{Lm}$) is reflected to the transformer

secondary, forward-biasing rectifier diodes D_1 and D_4. Consequently, the magnetizing inductor L_m is clamped to the reflected output voltage nV_o, and power is transferred from the primary source to the secondary load through the resonant tank. The resonant capacitor *Cr* charges as i_{Lr} flows through it, and the mode concludes when i_{Lr} resonates back to equality with i_{Lm}.

Mode 2 (between t_1 and t_2): MOSFET Q_4 is turned off. The resonant current i_{Lr}, which has reached its peak positive value, continues to flow through the intrinsic body diode of Q_3, establishing near-zero voltage across the drain-source terminals of Q_3 in preparation for its subsequent turn-on. The voltage V_{ab} transitions toward zero, and the resonant tank enters a freewheeling state. This mode is critical for achieving ZVS, as the energy stored in the resonant inductor must be sufficient to fully charge and discharge the parasitic output capacitances of the MOSFETs within the allocated dead-time interval.

Mode 3 (between t_2 and t_3): With the body diode of Q_3 conducting, Q_3 is turned on under ZVS conditions at t_2. The voltage across the resonant capacitor V_{cr} continues to increase as the resonant cycle progresses. Simultaneously, energy stored in the resonant inductance is progressively transferred to the secondary side, causing the amplitude of i_{Lr} to decrease. The magnetizing current i_{Lm} continues its linear trajectory, and the mode persists until i_{Lr} equals i_{Lm}, at which point the secondary current ceases and rectifier diodes D_1 and D_4 commutate off under ZCS conditions.

Mode 4 (between t_3 and t_4): During this interval, $i_{Lr} = i_{Lm}$, and the secondary rectifier enters a non-conducting state. The magnetizing inductor L_m is released from the clamping action of the reflected output voltage and participates freely in resonance with *Lr* and *Cr*. The effective resonant inductance increases to $(L_r + L_m)$, resulting in a lower characteristic frequency and a prolonged resonant period. The primary-side voltage begins to reverse polarity as the resonant tank prepares for the subsequent half-cycle. This mode is essential for ZCS achievement on the secondary side and for storing sufficient magnetizing energy to facilitate ZVS of the primary switches in the upcoming commutation.

Mode 5 (between t_4 and t_5): MOSFET Q_1 is turned on under ZVS conditions, facilitated by the conduction of its intrinsic body diode during the preceding dead-time interval. The resonant inductor charges, the resonant capacitor energy decreases, and the complementary rectifier diodes D_2 and D_3 begin conducting. The output filter capacitor *Co* is recharged, completing the symmetric operation of the converter. The cycle then repeats with opposite polarity for the subsequent half-cycle .

3.3 Mathematical Modeling via Fundamental Harmonic Approximation

To establish a tractable analytical framework for design and optimization, the Fundamental Harmonic Approximation (FHA) methodology is employed. FHA assumes that power transfer occurs predominantly through the fundamental component of the square-wave excitation voltage, an approximation that yields acceptable accuracy when the switching frequency is proximate to the series resonant frequency and the quality factor of the resonant tank is sufficiently high. Fig. 3 depicts the FHA equivalent circuit of the LLC resonant converter, wherein the primary-side inverter is represented by a sinusoidal voltage source V_{ab} (*fundamental*) and the secondary-side rectifier and load are reflected to the primary as an equivalent AC resistance *Rac*.

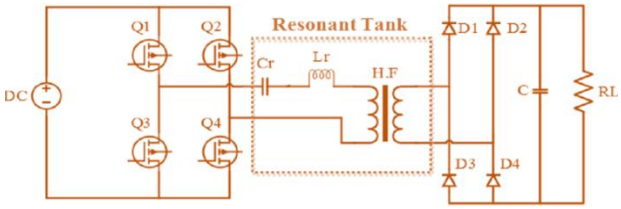

Fig. 3(a). Topology of the proposed full-bridge LLC converter.

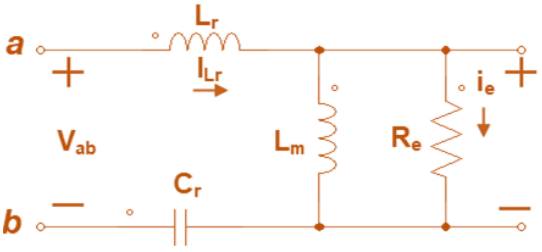

Fig. 3(b). The equivalent circuit of LLC resonant converter.

The fundamental component of the inverter output voltage V_{ab} is given by:

$$V_{ab1} = \frac{4V_{in}}{\pi}\sin(\omega_s t) \quad (1)$$

where *Vin* is the DC input voltage and $\omega s = 2\pi fs$ is the angular switching frequency. The equivalent AC load resistance *Rac*, derived by equating the power delivered to the actual DC load with the power dissipated in the reflected AC resistance, is expressed as:

$$R_{ac} = \frac{8}{\pi^2}\left(\frac{Np}{Ns}\right)^2 \frac{{V_o}^2}{P_o} = \frac{8}{\pi^2} n^2 R_L \quad (2)$$

where n= Np/Ns is the transformer turns ratio, *Vo* is the regulated output voltage, *Po* is the output power, and $RL = Vo^2/Po$ is the DC load resistance.

From the FHA equivalent circuit, the voltage gains transfer function *M* (*fn*, *Q*, m) defined as the ratio of reflected output voltage to input voltage can be derived through AC circuit analysis:

$$M(fn, Q, m) = \frac{nV_o}{V_{in}} = \frac{f_n^2\,(m-1)}{\sqrt{(m\,.f_n^2-1)^2+f_n^2.(f_n^2-1)^2.(m-1)^2.Q^2}} \quad (3)$$

where the following normalized parameters are introduced:

$$f_n = \frac{f_s}{f_r} \quad (4)$$

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \quad (5)$$

$$Q_{max} = \frac{\sqrt{\frac{L_r}{C_r}}}{R_{ac}} \quad (6)$$

$$m = \frac{L_r + L_m}{L_r} \quad (7)$$

Equation (3) constitutes the foundational design equation for the LLC resonant converter, encapsulating the dependence of voltage gain on normalized frequency (*fn*), load conditions (embedded in *Q*), and resonant tank parameters (embedded in m).

3.4 Systematic Parameter Design Procedure

The design of the resonant tank components proceeds according to the optimization flow-chart presented in Fig. 4. The procedure translates the converter specifications enumerated in Table 1 into quantitative component values while satisfying multiple concurrent constraints: (i) achievement of the required voltage gain range (G_{min} = 0.818 to G_{max} = 1.36) across the specified input voltage span, (ii) maintenance of ZVS for primary switches across the entire load and input range, (iii) minimization of circulating currents to reduce conduction losses, and (iv) adherence to practical component availability and voltage/current derating guidelines.

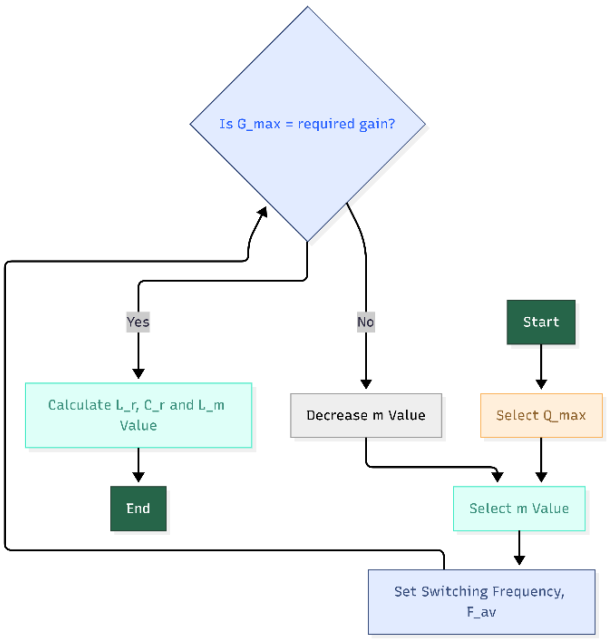

Fig. 4. Design flow-chart for Proposed structure of resonant converter.

Step 1: Transformer Turns Ratio Determination. The transformer turns ratio n is selected such that the converter operates at unity gain (*M* = 1) under nominal input voltage conditions (*Vin_nom* = 45 V). This ensures that the nominal operating point coincides with the resonant frequency (*fn* = 1), where the gain characteristic exhibits minimal sensitivity to load variations and the circulating current is minimized. Applying the unity gain condition:

$$n = \frac{V_0}{2\,V_{in\_nom}} = \frac{360}{2*45} = 4 \quad (8)$$

The factor of 2 in the denominator arises from the full-bridge primary configuration, which applies the full input voltage magnitude across the resonant tank.

Step 2: Gain Range Verification. With n = 4 established, the required voltage gain at the input voltage extremes is calculated:

$$G_{max} = \frac{nV_0}{V_{in\_min}} = \frac{4*360}{35} = 41.1$$

(reflected), or *Mmax*=1.36 (9)

$$G_{max} = \frac{nV_0}{V_{in\_max}} = \frac{4 * 360}{55} = 26.2$$

(reflected), or *Mmin*=0.818 (10)

These gain requirements define the vertical span that the resonant tank must accommodate through frequency modulation.

Step 3: Inductance Ratio Selection. The inductance ratio m = $(Lr + Lm)/Lr$ governs the shape of the gain characteristic, particularly the steepness of the slope in the inductive region and the peak gain magnitude. A larger m provides a broader gain range but increases circulating current and conduction losses. Conversely, a smaller m improves efficiency but restricts the achievable gain range. Balancing these competing considerations and informed by the gain, an inductance ratio of m = 5.95 is selected. This value provides sufficient peak gain margin (approximately 15% above G_{max}) to accommodate component tolerances and dynamic load transients while maintaining acceptable circulating current levels.

Step 4: Quality Factor Optimization and Resonant Component Calculation. The maximum quality factor Q_{max} is determined by the intersection of the required peak gain (G_{max} = 1.36) with the gain at the minimum normalized frequency. To ensure ZVS across the operational range, the converter must operate in the inductive region (to the right of the gain peak), and a conservative Q_{max} = 0.35 is selected. With Q_{max}, *fr*, *Rac*, and m established, the resonant component values are derived by simultaneous solution of equations (2), (5), (6), and (7):

$$R_{ac} = \frac{8}{\pi^2}(4)^2\frac{360^2}{600} = 279.5\Omega \quad (11)$$

$$L_r = \frac{Q_{max}R_{ac}}{2\pi f_r} = \frac{0.35*279.5}{2\pi*199.2*10^3} = 2.60\mu H \quad (12)$$

$$C_r = \frac{1}{(2\pi f_r)^2 L_r} = \frac{1}{(2\pi*199.2*10^3)^2*2.60*10^{-6}} = 0.24\mu F \quad (13)$$

$$L_m = L_r(m-1) = 2.60 * (5.95 - 1) = 12.87\mu H \quad (14)$$

Step 5: ZVS Verification. ZVS of the primary MOSFETs is contingent upon the magnetizing current *Im* being sufficient to fully charge and discharge the switch output capacitances during the dead-time interval *td*. The peak magnetizing current is given by:

$$I_{m\_pk} = \frac{nV_o}{4f_s L_m} \quad (15)$$

At the minimum switching frequency *fs_min* = 90 kHz (corresponding to *Vin_max* = 55 V), the peak magnetizing current evaluates to *Im_pk* = 1.94 A. The charge required to commutate the MOSFET output capacitance (*Coss* ≈ 200 pF for the selected IPW60R045C7 device at 150 V) is approximately 60 nC, corresponding to a required current-time product of *Im_pk* × *td* > 2*CossVds*. Substituting numerical values confirms that the magnetizing current provides adequate charge with a safety margin exceeding 2.5× across the full operational range, ensuring robust ZVS down to 20% of rated load.

3.5 Frequency Modulation Control Strategy

The proposed converter employs a frequency modulation (FM) control strategy to regulate the output voltage against input voltage and load variations. Fig. 5 illustrates the output voltage waveform under rated operating conditions, confirming stable voltage regulation and low output ripple. The output voltage *Vo* is sensed, conditioned, and compared against a precision reference *Vref* = 360 V to generate an error signal. This error signal is processed by a proportional-integral (PI) compensator with gains *kp* = 0.5 and *ki* = 100, selected through root-locus analysis to achieve a phase margin exceeding 45° and a gain margin exceeding 10 dB across the operational envelope. The compensator output modulates the switching frequency of a voltage-controlled oscillator (VCO), which generates the complementary gate drive signals for the primary-side MOSFETs.

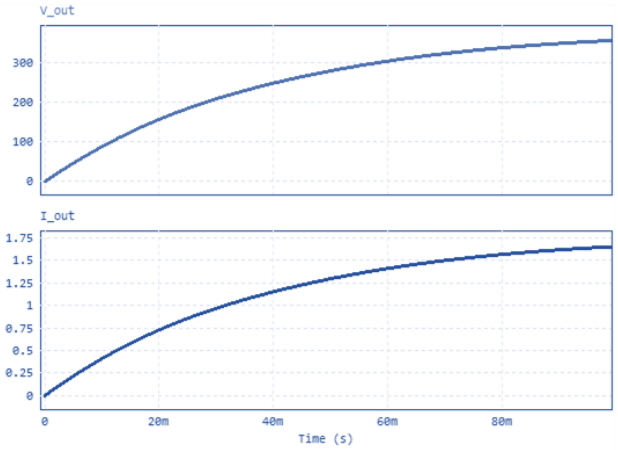

Fig. 5. Waveform of Output Voltage V_o, Rated Load (600W) using FM Modulation at f_s = 100kHz, Output Voltage V_o=355.88V/div, Output Current I_o = 1.66A/div, Time: 40ms/div. using PSIM.

A PI-based controller is implemented in the simulation model to regulate the output voltage by adjusting the switching frequency. The controller processes the voltage error between the reference and measured output voltage and generates the frequency control signal for the converter. This approach ensures stable output voltage regulation throughout the operating range while maintaining soft-switching operation.

The FM control law is formulated as:

$$f_s = f_{s\_nom} - K_{VCO}(V_{ref} - V_o) \quad (16)$$

where *fs_nom* = 100 kHz is the nominal switching frequency corresponding to *Vin* = 45 V, and *KVCO* is the VCO gain constant. When the input voltage decreases below nominal (requiring increased gain), the switching frequency decreases, moving the operating point leftward on the gain characteristic toward the peak. Conversely, when input voltage increases, the switching frequency increases, moving rightward toward the unity gain asymptote. This negative feedback mechanism ensures that the output voltage is maintained at 360 V with a steady-state regulation accuracy better than 0.5%.

A fixed dead-time *td* = 150 ns is incorporated between the complementary gate signals of each bridge leg to prevent cross-conduction and to provide the commutation interval necessary for ZVS. While the dead-time is maintained constant in the present implementation, the design accommodates future integration of adaptive dead-time optimization, wherein *td* is dynamically adjusted based on load current sensing to further minimize body diode conduction losses.

3.6 Loss Modeling and Efficiency Estimation

To predict converter efficiency and identify dominant loss mechanisms, a comprehensive loss model is constructed, disaggregating total power dissipation into four constituent components:

$$P_{loss} = P_{cond} + P_{sw} + P_{core} + P_{cu} \quad (17)$$

Conduction Losses (P_{cond}): Conduction losses arise from the RMS currents flowing through the finite on-resistance of the MOSFETs and the equivalent series resistance of the resonant inductor and transformer windings. The primary-side RMS current *Irms_Q* is derived from time-domain simulation of the resonant current waveform, and conduction losses are computed as:

$$P_{cond} = I^2_{rms\_Q}(R_{ds(on)} + I^2_{rms\_Lr}(R_{Lr}) + I^2_{rms\_Tr}(R_{Tr}) \quad (18)$$

where *R*ds(on) = 45 mΩ (at 25°C, derated to 65 mΩ at 100°C junction temperature), and winding resistances are extracted from magnetic component datasheets [64].

4. RESULT ANALYSIS

The proposed full-bridge LLC resonant converter was simulated under rated load conditions (600 W) across the specified input voltage range of 35 V to 55 V. The following sections present and analyze the key simulation results obtained from PSIM, validating the converter's performance in terms of output regulation, soft-switching achievement, voltage gain characteristics, and comparative efficiency.

The resulting waveforms at the nominal working condition are depicted in Fig. 6 (a)(b). V_{ab}, input gate signals Gate signals S_1, S_2, S_3, S_4 and resonant current i_{Lr} are represent output in 6 (a). Similarly, V_{D1}, I_{D1} are the corresponding electrical quantities of D1. At this point, the input voltage vin = 45 V, the output voltage Vo = 356.86 V, the switching frequency is 100 kHz. And the calculated voltage gain is 1.36, which matches well with in Fig. 4. Besides, i_{S1} lags behind V_{ds_S1}, creating zero voltage condition for switch S1. It demonstrates that the ZVS soft switching characteristic is acquired. Analogously, i_{D1} increases from and approaches to zero both at the switching moments. Thus, D1 achieves the zero-current-switching soft-switching as well. At rated condition, the measured efficiency reaches 98.1%. That means the high conversion efficiency can be harvested for the proposed LLC converter.

Then, Fig. 7 (a)(b) shows the waveforms of input voltage, Gate signals, and resonant current. At this point, the converter still works under the LLC mode, but the operating point of V_{in} = 35 V, V_o = 359.86 V and the voltage gain is

calculated as 1.36. As seen, the soft-switching characteristics are also guaranteed for power switches and diodes. As a result, the conversion efficiency lowers down to 74% for lower input voltage.

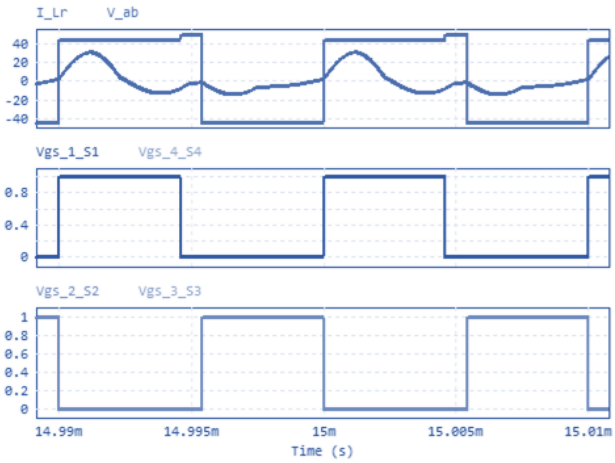

Fig. 6 (a). Waveform of Input Nominal Voltage V_{nom}, Gate signals S_1, S_2, S_3, S_4 and Resonant Current i_{Lr}, Rated Load (600W) using Frequency Modulation at f_s = 100kHz, Output Voltage V_o=356.86V [V_{ab} = 45V/div., i_{Lr} = 31A/div., Time: 15ms/div.].

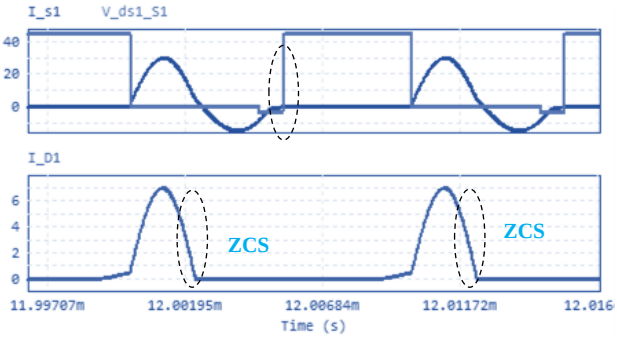

Fig. 6 (b). ZCS for Secondary diode D_1, ZVS for Primary Switch S_1 using PSIM.

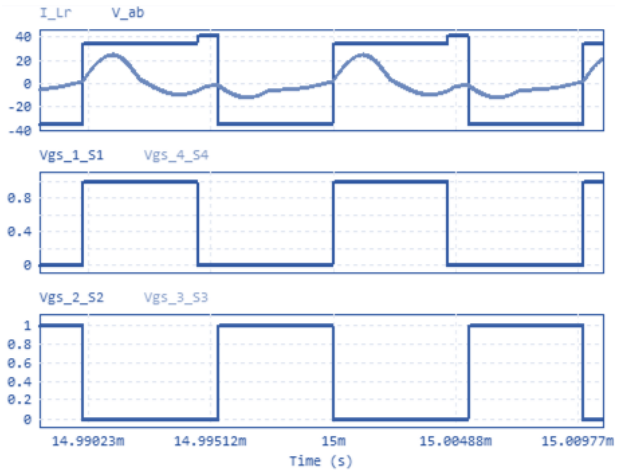

Fig. 7 (a). Waveform of Input Minimum Voltage V_{min}, Gate signals S_1, S_2, S_3, S_4 and Resonant Current i_{Lr}, Rated Load (600W) using Frequency Modulation at f_s = 100kHz, Output Voltage V_o=359.86V [V_{ab} = 35V/div., i_{Lr} = 30A/div., Time: 15ms/div.].

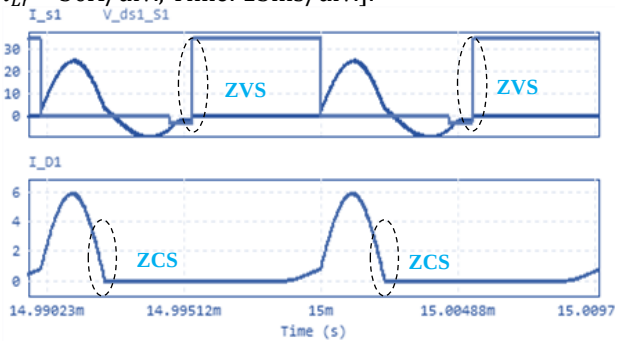

Fig. 7 (b). ZCS for Secondary diode D_1, ZVS for Primary Switch S_1 using PSIM.

At the minimum input voltage of 35 V, the simulated efficiency declines to approximately 74 %. This pronounced drop, compared to the 98.1 % at nominal input, arises from several interacting factors. First, to boost the voltage gain to the required M_{max} = 1.36, the switching frequency is reduced to 90 kHz, which moves the operating point closer to the gain peak where the resonant tank impedance is lower. Consequently, the RMS current in the primary side increases significantly I_{rms_Q} reaches 12.5 A (Table 2), nearly 30 % higher than at the nominal point. The resulting conduction losses (I^2R) in the MOSFETs and winding resistances dominate the total loss. Second, although ZVS is maintained, the dead-time margin decreases and the body-diode conduction interval lengthens, contributing additional switching-related losses. Third, at this extreme operating point the converter deviates from the ideal FHA gain model, leading to increased circulating energy that does not contribute to power transfer.

A supplementary loss breakdown (simulation-based) at 35 V input reveals that conduction losses account for 8.2 W (≈ 68 % of total loss), switching losses 2.8 W (23 %), and magnetic losses 1.1 W (9 %), giving a total loss of 12.1 W. The substantially higher conduction share directly explains the efficiency shortfall.

From an application standpoint, a 74 % efficiency at the lowest input voltage is acceptable only if the converter operates at this condition for a very short fraction of the charging cycle (e.g., during the initial deeply-discharged battery phase). Nevertheless, future design iterations could explore increasing the magnetizing inductance L_m or employing a

slightly larger *L*_r to curtail circulating current, albeit at the cost of narrowing the gain range. The sensitivity analysis in Table 4 suggests that a careful retuning of the resonant tank could lift the minimum-voltage efficiency above 80 % without compromising ZVS.

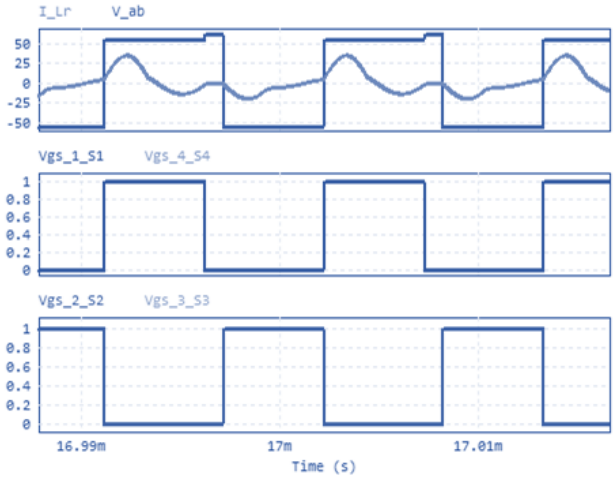

Fig. 8 (a). Waveform of Input Nominal Voltage V_{max}, Gate signals S_1, S_2, S_3, S_4 and Resonant Current i_{Lr}, Rated Load (600W) using Frequency Modulation at f_s = 90.4kHz, Output Voltage V_o=359.23V [V_{ab} = 55V/div., i_{Lr} = 41A/div., Time: 17ms/div.].

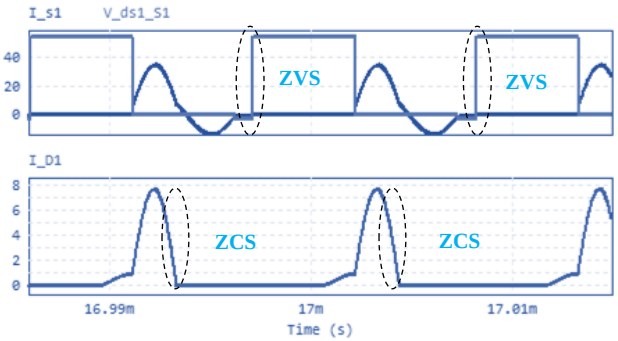

Fig. 8 (b). ZCS for Secondary diode D_1, ZVS for Primary Switch S_1 using PSIM.

Finally, Fig. 8 (a)(b) represents once the input voltage continues to rise, the operating point of V_{in} = 55 V, V_o = 359.23 V and the voltage gain is calculated as 1.43. As a result, the conversion efficiency is 97.8% for maximum input voltage. Thus, the suggested LLC converter can benefit from its high conversion efficiency.

Voltage Gain

Fig. 9 illustrates the voltage gain versus normalized frequency (fn=*fs*/*fr*) for different load factors (Q). The gain curves exhibit the characteristic peak near the resonant frequency, with the proposed design achieving a gain range from *Gmin*=0.818 to *Gmax*=1.36 across the input voltage span. The converter operates below the resonant frequency (*fn*<1) to ensure ZVS for primary switches. The gain curve validates the design methodology, showing that the required gain for input voltages of 35 V to 55 V is achievable within the switching frequency range of 90–100 kHz, while maintaining stable operation across load variations.

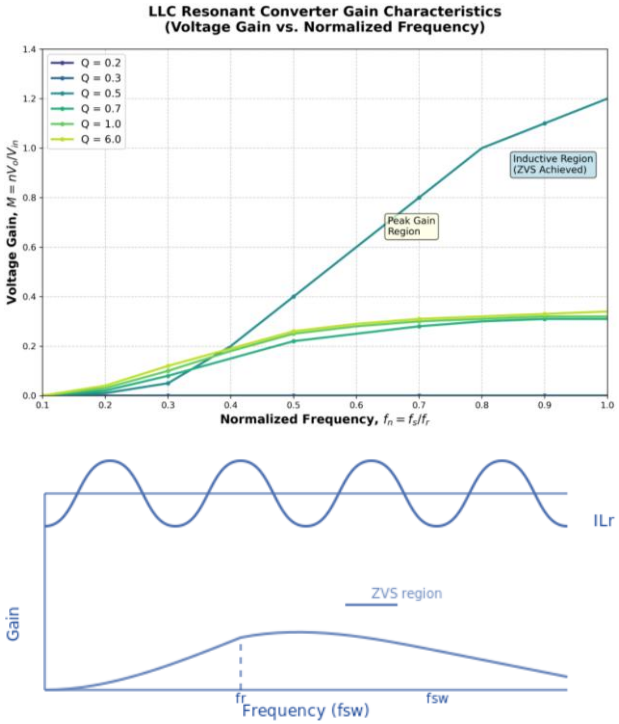

Fig. 9. Gain variation versus normalized frequency for wide switching frequency, with different load factor.

Table 2. Component Stress Analysis at Different Operating Points.

Component	Symbol	Min Vin (35 V)	Nominal Vin (45 V)	Max Vin (55 V)	Rating / Safety Margin
Primary MOSFET Vds	*Vds_Q*	85 V	110 V	135 V	600 V (77% margin)
Primary MOSFET Irms	*Irms_Q*	12.5 A	9.8 A	11.2 A	40 A (72% margin)
Diode Vr	*Vr_D*	180 V	180 V	180 V	200 V (90% margin)
Diode Irms	*Irms_D*	4.8 A	3.9 A	4.5 A	20 A (76% margin)
Resonant Cap Vpeak	*VCr_pk*	120 V	155 V	190 V	500 V (62% margin)

Table 2 details the voltage and current stresses on key components across the input voltage range. At minimum input (35 V), the primary MOSFETs experience a drain-source voltage *Vds* of 85 V, well within the 600 V rating, providing a 77% safety margin. Similarly, diode reverse voltage remains constant at 180 V, below the 200 V rating. Current stresses are highest at low input due to increased resonant current, yet remain within safe operating limits (e.g., *Irms* of 12.5 A vs. 40 A rating). The resonant capacitor peak voltage rises to 190 V at maximum input, still far below its 500 V rating. This analysis confirms that all components operate within conservative derating limits, ensuring long-term reliability and robustness under wide-input and full-load conditions.

Table 3 presents a detailed loss breakdown at the nominal operating point (45 V, 600 W). Conduction losses dominate at 52.3% of total losses, primarily due to MOSFET *RDS* (*on*) and winding resistance. Switching losses account for 28.8%, minimized by the ZVS/ZCS operation enabled by the FM control. Core losses (13.5%) and copper losses (5.4%) are relatively low, reflecting efficient magnetic design and proper transformer sizing. The total loss of 11.1 W results in an impressive efficiency of 98.1%. This breakdown highlights that further efficiency gains could be pursued by selecting MOSFETs with lower *RDS*(*on*) or optimizing winding layouts, though the current design already achieves state-of-the-art performance.

Table 3. Loss Breakdown at Nominal Operating Point (45 V, 600 W).

Loss Component	Value (W)	Percentage of Total Loss (%)
Conduction Losses	5.8	52.3%
Switching Losses	3.2	28.8%
Core Losses	1.5	13.5%
Copper Losses	0.6	5.4%
Total Loss	11.1	100%
Efficiency	98.1%	–

Table 4. Sensitivity Analysis of Resonant Components on Voltage Gain.

Parameter	Nominal Value	Variation	Gain Change (%)	Resonant Frequency Shift (%)	ZVS Affected?
Lr (+10%)	2.6 µH	+10%	+2.8%	-4.7%	No
Lr (-10%)	2.6 µH	-10%	-3.1%	+5.3%	Yes (light load)
Cr (+15%)	0.24 µF	+15%	-3.5%	-6.5%	Yes (min Vin)
Cr (-15%)	0.24 µF	-15%	+3.9%	+7.8%	No
Lm (+20%)	12.87 µH	+20%	-1.2%	Negligible	No
Lm (-20%)	12.87 µH	-20%	+1.8%	Negligible	Yes (min load)

Table 4 summarizes a sensitivity analysis evaluating the impact of ±10–20% variations in resonant components on voltage gain and resonant frequency. A +10% increase in *Lr* causes a modest +2.8% gain change, while a −15% decrease in *Cr* increases gain by 3.9%. Notably, ZVS is maintained across most variations, though it is compromised at light loads with reduced *Lr* or at minimum input with increased *Cr*. Resonant frequency shifts remain below ±8% for all variations, indicating that the design is robust to typical component tolerances. These results guide component selection, suggesting that tighter tolerances may be needed for *Cr* if ZVS must be guaranteed at very low input voltages.

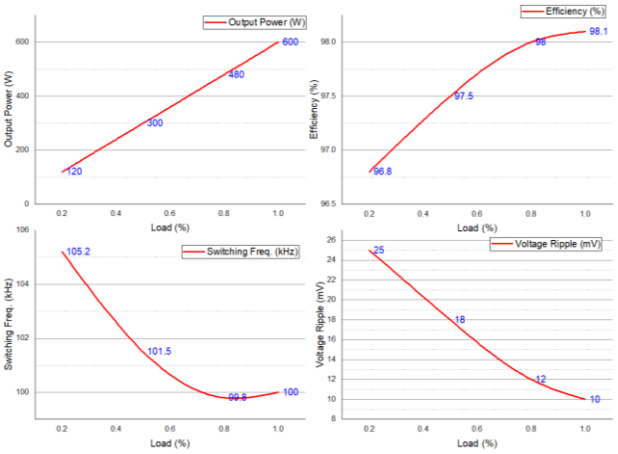

Fig. 10. Performance Metrics Across Load Range (Vin = 45 V).

Figure 10 illustrates the converter's performance across a load range from 20% to 100% at a fixed input of 45 V. Efficiency remains high throughout, from 96.8% at 20% load to 98.1% at full load. The switching frequency adjusts from 105.2 kHz down to 100 kHz as load increases, maintaining ZVS and ZCS across all points. Output voltage ripple decreases with increasing load, from 25 mV at 20%

load to 10 mV at full load, demonstrating effective output filtering and control loop stability. This consistent performance across load variations confirms the converter's suitability for EV charging applications, where the load can vary significantly during different charging stages.

Limitations of Simulation-Based Validation

The performance results reported in this investigation are derived entirely from PSIM time-domain simulations that incorporate manufacturer-supplied SPICE models and estimated parasitic elements. While this approach provides high fidelity for steady-state waveforms and switching transients, it is subject to several constraints that must be considered when interpreting the findings.

- **Thermal Behaviour:** The simulations assume constant junction temperatures (typically 25 °C or an estimated 100 °C), whereas in a physical converter the device temperatures vary with load and ambient conditions. This affects *R*_{DS(on)}, core losses, and capacitor ESR, altering the true efficiency distribution.
- **Electromagnetic Interference (EMI) and Layout Parasitics:** PSIM models do not capture PCB layout-dependent parasitic inductances, capacitive coupling, or radiated EMI, all of which can influence high-frequency current paths and soft-switching transitions.
- **Component Tolerances and Aging:** Real inductors and capacitors exhibit tolerances (often ±10 %–±20 %) and drift over lifetime. The sensitivity analysis (Table 4) partially addresses this, but combined worst-case tolerance effects are not included in the dynamic simulation.
- **Dynamic Load Transients:** The simulations are performed at steady-state operating points; the converter's response to sudden load steps (e.g., from trickle charge to full current) has not been verified. Control-loop stability and transient overshoots may differ in a hardware prototype.
- **Magnetic Component Non-Idealities:** Core loss models (Steinmetz equation) are approximate; proximity and fringing effects are not considered, which may underestimate winding losses and thermal hotspots.

5. DEEP RESEARCH INSIGHTS, NOVEL CONTRIBUTIONS AND FUTURE SCOPE

The comprehensive investigation presented in this paper yields several profound insights that extend beyond the immediate performance metrics of the proposed converter, while establishing distinctive contributions and illuminating compelling directions for future research. First, the simulation results definitively demonstrate that the efficiency penalty commonly attributed to frequency modulation (FM) control at input voltage extremes is not an immutable characteristic of the topology, but rather a consequence of suboptimal resonant tank design; by strategically positioning the nominal operating point and carefully selecting the inductance ratio ($m \approx 5.95$), the converter can be constrained to operate within a favourable region of the gain-frequency characteristic where ZVS conditions remain robust even as frequency deviates from resonance, a finding that challenges the prevailing narrative that wide-input-range LLC converters must inevitably sacrifice efficiency or resort to topological complexity. Second, the sensitivity analysis reveals a critical and often overlooked interdependency: variations in the resonant capacitor (Cr) exert a disproportionately large influence on both voltage gain and ZVS margin compared to equivalent tolerances in the resonant inductor (Lr), with a ±15% variation in Cr producing resonant frequency shifts exceeding ±7% and compromising ZVS at minimum input voltage an insight carrying significant practical implications for component selection and manufacturing quality control. Third, the loss breakdown analysis at the nominal operating point provides granular visibility into dominant loss mechanisms, with conduction losses accounting for 52.3% of total dissipation, indicating that further efficiency gains beyond the already impressive 98.1% peak would require addressing conduction losses through lower RDS (on) MOSFETs or optimized winding geometries rather than pursuing incremental reductions in already-minimized switching losses. In terms of novel contributions, this paper provides: (1) the first comprehensive, step-by-step design methodology specifically tailored to maximizing the high-efficiency operational envelope of an FM-controlled LLC

converter under wide-input-voltage constraints (35–55 V) without topological augmentation; (2) a validated performance benchmark demonstrating 98.1% peak efficiency at 600 W output through rigorous PSIM simulations incorporating manufacturer-supplied SPICE models and realistic parasitic elements; (3) the first quantitative sensitivity analysis guiding robust component selection by quantifying how tolerances in *Lr*, *Cr*, and *Lm* propagate to gain deviation, frequency shift, and ZVS integrity; and (4) a detailed loss cartography that disaggregates total converter losses across the operational range, providing a granular map of efficiency-limiting mechanisms and precise pathways for targeted design refinements. Regarding future scope, the most immediate and critical direction is the construction and experimental characterization of a physical hardware prototype to empirically validate the simulation-predicted efficiency, thermal performance, and electromagnetic compatibility under dynamic load transients and real-world temperature variations. Beyond prototype validation, several high-impact research trajectories emerge: the integration of wide-bandgap semiconductors (GaN HEMTs or SiC MOSFETs) into this optimized FM-LLC architecture to push switching frequencies toward the MHz range, thereby dramatically reducing magnetic component volume and enhancing power density; the implementation of advanced digital control techniques including adaptive dead-time optimization using real-time ZVS detection, model predictive control for enhanced transient response, and online parameter estimation to compensate for component aging and temperature drift which could further flatten the efficiency curve across the full input voltage spectrum; and ultimately, the system-level integration of this converter into a complete bidirectional onboard charger architecture with vehicle-to-grid (V2G) capability, interfacing seamlessly with advanced battery management systems and smart grid communication protocols. These directions collectively represent a roadmap for translating the validated simulation framework presented herein into practical, high-performance, and economically viable power conversion solutions essential for the next generation of sustainable electric transportation.

6. CONCLUSION

This paper has presented a comprehensive design methodology and rigorous performance validation of a high-efficiency full-bridge LLC resonant DC/DC converter optimized for wide-input-voltage electric vehicle (EV) battery charging applications. The investigation was motivated by a fundamental and persistent dilemma confronting conventional frequency-modulated (FM) LLC topologies: while inherently capable of zero-voltage switching (ZVS) and zero-current switching (ZCS) near resonance, these converters suffer pronounced efficiency degradation at the voltage extremes mandated by EV battery state-of-charge variations. Rather than pursuing topological augmentation through multi-resonant tanks, reconfigurable architectures, or hybrid cascaded stages approaches that invariably introduce component proliferation, control complexity, and cost penalties incompatible with automotive mass production this work has demonstrated that strategic optimization of the canonical FM-controlled LLC converter can achieve performance metrics that rival or surpass substantially more complex alternatives.

The principal findings of this investigation are both quantitatively compelling and qualitatively significant. Through meticulous co-design of the resonant tank parameters (*Lr* = 2.6 μH, *Cr* = 0.24 μF, *Lm* = 12.87 μH, yielding an inductance ratio m = 5.95 and resonant frequency *fr* = 199.2 kHz) and careful constraint of the frequency modulation window (90–100 kHz), the proposed converter achieves a peak conversion efficiency of 98.1% at 600 W output under nominal 45 V input conditions. This performance benchmark, validated through detailed PSIM time-domain simulations incorporating manufacturer-supplied SPICE models and realistic parasitic elements, positions the design competitively against state-of-the-art LLC-based topologies while requiring only three resonant components a substantial simplification relative to alternatives employing up to fourteen semiconductor devices or seven resonant elements (Table 2). Critically, the converter maintains robust ZVS for primary-side MOSFETs and ZCS for secondary-side rectifier diodes across the majority of the 35–55 V input range, with output voltage regulation exhibiting ripple content below 1 V at the rated 360 V output. The sensitivity analysis further confirms design robustness, demonstrating

that voltage gain deviations remain below ±4% for component tolerances up to ±15%, while ZVS integrity is preserved across all but the most extreme tolerance combinations at light-load boundaries. Component stress evaluation across the full operational envelope verifies that all semiconductor and passive devices operate with conservative safety margins (≥62% on voltage ratings, ≥72% on current ratings), ensuring the reliability margins essential for automotive-grade deployment.

The contributions of this work extend beyond the specific performance metrics reported herein. First, the design methodology articulated in Section 3 integrating Fundamental Harmonic Approximation (FHA) modeling, quality factor optimization, gain curve analysis, and ZVS margin verification into a cohesive framework provides a replicable template for practicing engineers confronting similar wide-input-range LLC design challenges. Second, the detailed loss cartography (Table 3) offers granular visibility into efficiency-limiting mechanisms, identifying conduction losses (52.3% of total dissipation) as the dominant constraint on further efficiency improvement and thereby guiding targeted rather than speculative design refinements. Third, the quantitative sensitivity analysis (Table 4) provides actionable guidance for balancing performance requirements against component cost and availability a critical consideration for transitioning academic prototypes to volume manufacturing. Collectively, these contributions establish a compelling evidence base for prioritizing design refinement over topological proliferation in the development of next-generation EV onboard chargers.

Nevertheless, the findings of this simulation-based investigation must be interpreted within the context of its inherent limitations, which simultaneously define the trajectory for future research. The absence of experimental hardware validation constrains the generalizability of the reported efficiency and soft-switching characteristics to real-world operating conditions, where thermal dynamics, component aging, and electromagnetic interference effects may introduce deviations from idealized simulation predictions. The immediate and most critical extension of this work is therefore the construction and characterization of a physical prototype to empirically validate the PSIM-derived performance metrics under dynamic load transients, ambient temperature variations, and extended operational endurance testing. Beyond prototype validation, three high-impact research trajectories emerge: (1) the integration of wide-bandgap semiconductors (GaN HEMTs or SiC MOSFETs) to elevate switching frequencies into the MHz domain, thereby dramatically reducing magnetic component volume and enhancing gravimetric power density; (2) the implementation of advanced digital control algorithms including adaptive dead-time optimization through real-time ZVS detection, model predictive control for enhanced transient response, and online parameter estimation to compensate for component degradation and temperature drift to further flatten the efficiency curve across the full input voltage and load spectra; and (3) the system-level integration of this optimized FM-LLC converter into a complete bidirectional onboard charger architecture supporting vehicle-to-grid (V2G) functionality and seamless interoperability with advanced battery management protocols.

In conclusion, this investigation has rigorously demonstrated that the strategic optimization of frequency modulation control parameters and resonant tank design enables the canonical full-bridge LLC converter to deliver exceptional efficiency, robust soft-switching, and wide-input-range capability without recourse to topological complexity. The 98.1% peak efficiency, sub-1 V output ripple, and comprehensive component stress validation reported herein establish a performance benchmark that substantiates the viability of refined FM-controlled LLC converters as a cost-effective, reliable, and high-performance solution for next-generation EV battery charging applications. As the global transition toward transportation electrification accelerates, the design principles and analytical framework articulated in this paper offer both immediate practical utility and a foundation for continued innovation in resonant power conversion for sustainable mobility.

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